REMARKS

This Application has been carefully reviewed in light of the Final Office Action mailed February 17, 2010. In the Final Office Action, all pending Claims 1-20 were rejected. Independent Claims 1 and 20 are herein amended. Applicants respectfully request reconsideration and allowance of all Claims 1-20.

Rejections under 35 U.S.C. § 112

Claims 1-20 were rejected by the Examiner under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement, specifically regarding the phrase "a breach of the protective layer." Although Applicants disagree, Applicants have herein amended independent Claims 1 and 20 to remove the objected-to phrase.

Amended Independent Claims 1 and 20 are Allowable

Independent Claims 1 and 20 were rejected under 35 U.S.C. §103(a) as being obvious in view of *Yamauchi* (U.S. Patent Publication 2002/0040420), *Anderson* (U.S. Patent Publication 2003/0084336), and *Rollender* (U.S. Patent 5,842,571).

In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Even if each limitation is disclosed in a combination of references, however, a claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. *KSR Int'l. Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007). Rather, the Examiner must identify an apparent reason to combine the known elements in the fashion claimed. *Id.* "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*, citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Finally, the reason must be free of the distortion caused by hindsight bias and may not rely on ex post reasoning. *KSR*, 127 S.Ct. at 1742. In addition, evidence that such a combination was uniquely challenging or difficult tends to show that a claim was not obvious. *Leapfrog*

Enterprises, Inc. v. Fisher-Price, Inc. and Mattel, Inc., 485 F.3d 1157, 1162 (Fed. Cir. 2007), citing *KSR*, 127 S.Ct. at 1741.

Applicants submit that *Yamauchi*, *Anderson*, and *Rollender*, whether considered alone or in combination, do not teach all limitations of amended Claims 1 and 20. For example, amended independent Claims 1 and 20 recite:

> a security sensor system including a ***protective layer on the integrated circuit including at least one elongated electrical line extending along the surface of the integrated circuit***, the security sensor system operable to monitor the state of the protective layer on the integrated circuit such that ***when a breaking of the electrical line is detected, data is automatically deleted from at least one memory of the integrated circuit***.

Yamauchi, *Anderson*, and *Rollender* all fail to teach these limitations. In particular, as discussed below, none of *Yamauchi*, *Anderson*, and *Rollender* teach (a) a protective layer including at least one elongated electrical line extending along the surface of an integrated circuit, or (b) when a breaking of an electrical line of a protective layer is detected, automatically deleting data from memory on the integrated circuit.

Yamauchi. The Examiner acknowledges that *Yamauchi* does not teach monitoring the state of a protective layer on an integrated circuit (Final Office Action, page 4).

Anderson. The Examiner alleges that paragraphs 0008 and 0014 of *Anderson* teaches monitoring the state of a protective layer on an integrated circuit. (Office Action, page 5). Applicants respectfully disagree, and moreover, submit that *Anderson* does not teach *a protective layer having an elongated electrical line, which is monitored to detect a break in the electrical line*. Paragraph 0008 teaches:

> [0008] Our invention is adapted from dual-rail encoded asynchronous logic because in this technology, the power consumed can be made substantially independent of the data being processed, and by the choice of suitable design rules, which should be clear to those skilled in the art, the design can be made resistant to single-transistor and single-wire faults. Furthermore, such circuits are already known to be highly resilient to

> variations in the applied power supply voltage. In our invention, alarms resulting from environmental sensors or from the activation of other protective mechanisms can be propagated rapidly through the chip using many independent paths.

Applicants assume the Examiner is referring specifically to the passage teaches "alarms resulting from environmental sensors or from the activation of other protective mechanisms can be propagated rapidly through the chip using many independent paths." However, the passage merely teaches activation of protective mechanisms in general, but does not disclose the specific protective mechanism recited in Applicants' amended claims -- namely, ***a protective layer having an elongated electrical line, which is monitored to detect a break in the electrical line***. Further, the passage certainly does not teach *automatically deleting data* from memory on the integrated circuit when a break in the electrical line of the protective layer is detected.

Paragraph 0014 of *Anderson* teaches:

> [0014] A processor pipeline with a quad-coded data-path may be constructed using well known dual-rail pipelining techniques [3]. Alarm signals can be inserted using an OR function of the data and with a sense signal from a sensor (see FIG. 1). One sensor in our invention is based on an instruction counter; the processor software can check that the expected number of instructions have been executed and alarm if this is riot [sic] the case (as might happen, for example, under destructive probing attack). In the single circuit implementing the instruction by which this alarm is executed, we depart from the quad-coded logic rules described herein so that an alarm hardware state may be generated from a non-alarm hardware state. Other sensors are outside the scope of this patent but may typically be designed to detect out-of-bounds environmental parameters such as over- and under-voltage and low temperature. This OR function can be combined with the combinational function indicated to assist the usual gate minimisation process.

Like paragraph 0008 discussed above, paragraph 0014 does not teach anything about a ***protective layer*** on the integrated circuit, much less ***a protective layer having an elongated electrical line, which is monitored to detect a break in the electrical line***, much less *automatically deleting data* from memory on the integrated circuit when a break in the electrical line is detected.

Rollender. The Examiner alleges that *Rollender* teaches automatically deleting data from memory of an integrated circuit when a breach of a protective layer is detected. (Final Office Action, pages 6-7). Specifically, the Examiner cites the following portions of *Rollender*: (a) col. 1, line 58 to col. 2, line 6; (b) Fig. 3; (c) col. 4, lines 6-33, (d) col. 4, lines 30-33; and (e) col. 2, lines 19-21. (Final Office Action, pages 6-7).

Applicants disagree. It is important to view each of the portions of *Rollender* in their proper context. *Rollender* teaches three types of embodiments:

(a) A prior art embodiment that includes IC layers surrounded by a hardened, brittle protective layer 30. (*see* col. 2, line 54 to col. 3, line 23);

(b) Embodiments of the invention that include IC layers fused directly to each other to provide data security, such that a protective layer is not needed. (*see* col. 1, line 54 to col. 2, line 6; and col. 3, lines 24 to col. 4, line 57); and

(c) Embodiments of the invention that include IC layers fused directly to each other to provide data security [similar to embodiments (b) above], and also including a hardened, brittle protective layer 30 [similar to prior art embodiment (a) above]. (*see* col. 4, line 58 to col. 5, line 14).

Each of these three embodiments is discussed below in further detail.

First, referring in more detail to the prior art embodiment (a) listed above, *Rollender* teaches a prior art security device that includes silicon layers 22 and 24 that are surrounded by a hardened, brittle protective layer 30. (col. 2, line 54 to col. 3, line 3). "Due to the brittleness of the protective layer 30, the silicon layers 22 and 24 themselves are destroyed when any significant violence is done to the package, including cutting or burning away of the protective layer 30." (col. 3, lines 3-7).

Thus, this is simply a teaching of the conventional brittle protective layer 30 that surrounds IC chips, where damaging the brittle protective layer 30 damages the encompassed IC chips. There is no teaching in *Rollender* that data is automatically erased from memory when damage to the protective layer 30 is detected.

Second, referring in more detail to the embodiments (b) listed above, *Rollender* teaches two IC layers 42 and 44 facing each other and fused directly to each other such that data is erased or destroyed when the IC layers are separated or when one of the IC layers is destroyed. Thus, for these embodiments, *Rollender* teaches "**There need be no protective layer 30: each silicon layer protects the other from inspection.**" (col. 3, lines 37-38). Thus, with respect to these embodiments, *Rollender* teaches away from using a protective layer, and certainly does not teach automatically erasing data from memory when damage to a protective layer is detected.

Third, referring in more detail to the embodiments (c) listed above, *Rollender* teaches two IC layers fused directly to each other to provide data security (similar to embodiments (a) above), and also including a hardened, brittle protective layer 30 (*see* similar to prior art embodiment (a) above). Thus, like the protective layer of the prior art, protective layer 30 of these embodiments is a hardened, brittle casing that surrounds the IC layers. Again, there is no teaching in *Rollender* that data is automatically erased from memory when damage to the protective layer 30 is detected.

Thus, none of these embodiments includes a ***protective layer*** that is monitored such that ***data is automatically erased from memory*** upon detecting damage to the protective layer. Further, even if *Rollender* did teach this feature (which it does not), *Rollender* certainly does not teach the specific features now recited in amended Claims 1 and 20 -- namely, ***a protective layer having an elongated electrical line, which is monitored to detect a break in the electrical line***, and ***automatically deleting data*** from memory on the integrated circuit ***when a break in the electrical line is detected***. *Rollender* does not teach a protective layer having an electrical line, much less detecting a break in an electrical line of a protective layer, much less automatically deleting data from memory upon detecting a break in an electrical line of a protective layer.

For at least the reasons discussed above, amended independent Claims 1 and 20 are allowable over the cited references. Therefore, Applicants respectfully request allowance of Claims 1 and 20, as well as all claims that depend from Claim 1.

All Dependent Claims are Also Allowable.

Dependent Claims 2-4, 6-8, and 10-11 were rejected under 35 U.S.C. §103(a) as being obvious in view of *Yamauchi*, *Anderson*, and *Rollender*.

Dependent Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Yamauchi*, *Anderson*, *Rollender*, and *Nakajima* (U.S. Patent Publication 2004/0106239).

Dependent Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Yamauchi*, *Anderson*, *Rollender*, and *Fricke* (U.S. Patent 6,711,045).

Dependent Claim 12 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Yamauchi*, *Anderson*, *Rollender*, and *Khoury* ((U.S. Patent Publication 2001/0053565).

Dependent Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Yamauchi*, *Anderson*, *Rollender*, and *Anthony* (U.S. Patent Publication 2003/0206388).

Dependent Claim 14 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Yamauchi*, *Anderson*, *Rollender*, and *Huttunen* (U.S. Patent Publication 2003/0147267).

Dependent Claim 16-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Yamauchi*, *Anderson* , *Rollender*, and *Kean* (U.S. Patent Publication 2001/0015919).

Dependent Claim 15 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Yamauchi*, *Anderson*, *Rollender*, *Huttunen*, and *Kean*.

Applicants submit that all dependent claims are allowable at least because they depend from independent Claim 1, which is shown above to be allowable. In addition, *Nakajima*, *Fricke*, *Khoury*, *Anthony*, *Huttunen*, and *Kean* also do not teach the limitations of Claim 1 discussed above, and the Examiner has not alleged that these references do teach anything similar to these limitations. Further, Applicants do not concede that any of the combinations of references proposed by the Examiner are legally proper.

Thus, for at least these reasons, Applicants respectfully request reconsideration and allowance of all dependent claims.

CONCLUSION

Applicants have made an earnest effort to place this case in condition for allowance in light of the remarks set forth above. Applicants respectfully request reconsideration of the pending claims.

Applicants believe there are no fees due at this time. However, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-4871 of King & Spalding L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512-457-2030.

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